Electronic Version

Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A method for implementing circuit layouts in a chip, comprising:

forming a plurality of sub-circuit cells with the same layout in different positions of the chip; and

when the sub-circuit cells in different positions require different circuit functions, performing a layout programming in at least a connection layer so that different layouts are formed in different positions of the connection layer corresponding to the sub-circuit cells.

[c2] 2.The method of claim 1, wherein the connection layer is a metal layer.

[c3] 3.The method of claim 1, the layout programming is only performed in the connection layer so that the sub-circuit cells with different circuit functions have different layouts only in the connection layer.

[c4] 4.The method of claim 1, wherein while forming the plurality of sub-circuit cells with the same layout, a plurality of sub-circuit blocks are laid in each sub-circuit cell, wherein while performing the layout programming, each

layout in the connection layer corresponding to each sub-circuit cell is selectively connected to the sub-circuit blocks of each sub-circuit cell so that the sub-circuit cells in different positions implement different circuit functions.

[c5] 5.The method of claim 1, wherein the sub-circuit cells in different positions are for implementing input/output (I/O) circuits with different I/O functions.

[c6] 6.The method of claim 5, wherein the sub-circuit cells in different positions are for implementing I/O circuits with a Schmidt trigger function.

[c7] 7.The method of claim 5, wherein the sub-circuit cells in different positions are for implementing I/O circuits with different slew rates.

[c8] 8.The method of claim 5, wherein the sub-circuit cells in different positions are for implementing I/O circuits with different driving currents.

[c9] 9.A chip, comprising:

a plurality of layout layers comprising a plurality of same layouts in a plurality of positions of the layout layers so as to implement a plurality of sub-circuit cells with the same layout; and

at least a connection layer comprising different layouts

corresponding to the different positions of the layout layers so that the sub-circuit cells in different positions implement different circuit functions.

[c10] 10.The chip of claim 9, wherein the connection layer is a metal layer.

[c11] 11.The chip of claim 9, wherein each sub-circuit cell comprises a plurality of sub-circuit blocks, and the lay-outs of the connection layer are selectively connected the sub-circuit blocks of each sub-circuit cell so that the sub-circuit cells in different positions implement differ-ent circuit functions.

[c12] 12.The chip of claim 9, wherein the connection layer im-plements input/output (I/O) circuits with different I/O functions by the sub-circuit cells in different positions.

[c13] 13.The chip of claim 12, wherein the connection layer implements I/O circuits with a Schmidt trigger function with the sub-circuit cells in different positions.

[c14] 14.The chip of claim 12, wherein the connection layer implements I/O circuits with different slew rates with the sub-circuit cells in different positions.

[c15] 15.The chip of claim 12, wherein the connection layer implements I/O circuits with different driving currents

with the sub-circuit cells in different positions.